

IN THE CLAIMS

1. (currently amended) A non-volatile synchronous memory device comprising:
an array of non-volatile memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of non-volatile memory cells; and
a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, wherein each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks and wherein the non-volatile synchronous memory device is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while accessing a second bank.
2. (original) The non-volatile synchronous memory device of claim 1 wherein the plurality of addressable banks comprise four addressable banks.
3. (currently amended) The non-volatile synchronous memory device of claim 1 further comprising control circuitry to copy data from a first row of ~~a first~~ the first bank of the plurality of addressable banks to a first buffer of the plurality of buffers.
4. (original) The non-volatile synchronous memory device of claim 3 wherein an address of the first row is predefined and the control circuitry copies the data in response to an externally provided command.
5. (original) The non-volatile synchronous memory device of claim 1 wherein the plurality of buffers can be read while data is written to the plurality of banks.
6. (currently amended) A processing system comprising:
a processor; and
a non-volatile synchronous memory device coupled to the processor and comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks,
each bank comprises addressable rows and columns of non-volatile memory cells,
and

a plurality of bank buffers, the bank buffers and addressable banks coupled one to
one, wherein each of the plurality of bank buffers is adapted to store data from a
row of memory cells contained in its corresponding addressable bank of the
plurality of addressable banks and wherein the non-volatile synchronous memory
device is adapted to simultaneously execute read and write operations on a first
bank of the plurality of addressable banks while executing a read, write, or erase
operation on a second bank.

7. (original) The processing system of claim 6 wherein the plurality of addressable banks comprise four addressable banks.
8. (currently amended) The processing system of claim 6 wherein the non-volatile synchronous memory device further comprises control circuitry to copy data from a first row of ~~a first~~ the first bank of the plurality of addressable banks to a first buffer of the plurality of buffers.
9. (original) The processing system of claim 8 wherein an address of the first row is predefined and the control circuitry copies the data in response to an externally provided command.
10. (original) The processing system of claim 6 wherein the plurality of buffers can be read while data is written to the plurality of banks.
11. (currently amended) A method of writing to a flash memory comprising:
copying first data stored in a row of a first non-volatile memory cell array bank to a first buffer circuit using control circuitry of the flash memory;
copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit using the control circuitry;

performing a write operation to write third data to the first array bank using a first external processor coupled to the flash memory;
reading the first data from the first buffer circuit using the first external processor while performing the write operation; and
reading the second data from the second array bank using a second external processor coupled to the flash memory while performing the write operation.

12. (original) The method of claim 11 further comprising:
monitoring a status of the flash memory to determine when the write operation is completed.
13. (previously presented) The method of claim 12 wherein monitoring is performed by the first external processor in response to the first data read from the buffer circuit.
14. (previously presented) The method of claim 11 wherein copying the first data is initiated by the first external processor coupled to the flash memory.
15. (previously presented) The method of claim 11 wherein copying the first data and performing the write operation is initiated by the first external processor coupled to the flash memory.
- 16-27. (cancelled)
28. (original) The non-volatile synchronous memory device of claim 4, wherein the externally provided command is a write command.
29. (original) The processing system of claim 9, wherein the externally provided command is a write command.
30. (original) The processing system of claim 6, further comprising:
a second processor coupled to the non-volatile synchronous memory device.

31. (original) The processing system of claim 30, wherein the non-volatile synchronous memory device is adapted to allow the second process to read data from a second bank of the array while the processor writes data to a first bank.
32. (original) The method of claim 14, wherein copying the first data is initiated by the first external processor coupled to the flash memory further comprises copying the first data is initiated by a write command from the first external processor coupled to the flash memory.
33. (currently amended) A flash memory device comprising:
an array of flash memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of flash memory cells; and
a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, wherein each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks and wherein the flash memory device is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while executing an access of a second bank.
34. (original) The flash memory device of claim 33, wherein the plurality of addressable banks comprise four addressable banks.
35. (currently amended) The flash memory device of claim 33, further comprises control circuitry to copy data from a first row of ~~a first~~ the first bank of the plurality of addressable banks to a first buffer of the plurality of buffers.
36. (original) The flash memory device of claim 35, wherein an address of the first row is predefined and the control circuitry copies the data in response to an externally provided command.

37. (original) The flash memory device of claim 33, wherein the plurality of buffers can be read while data is written to the plurality of banks.
38. (original) The flash memory device of claim 33, wherein the externally provided command is a write command.